

## TL08xx JFET-Input Operational Amplifiers

### 1 Features

- Low Power Consumption: 1.4 mA/ch Typical
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias Current: 30 pA Typical
- Low Input Offset Current: 5 pA Typical
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typical
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- High Slew Rate: 13 V/ $\mu$ s Typical
- Common-Mode Input Voltage Range Includes  $V_{CC+}$

### 2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

### 3 Description

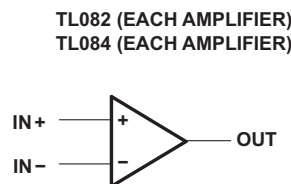
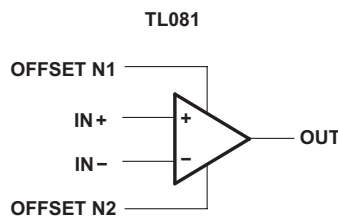
The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)    |
|-------------|------------|--------------------|
| TL084xD     | SOIC (14)  | 8.65 mm × 3.91 mm  |
| TL08xxFK    | LCCC (20)  | 8.89 mm × 8.89 mm  |
| TL084xJ     | CDIP (14)  | 19.56 mm × 6.92 mm |
| TL084xN     | PDIP (14)  | 19.3 mm × 6.35 mm  |
| TL084xNS    | SO (14)    | 10.3 mm × 5.3 mm   |
| TL084xPW    | TSSOP (14) | 5.0 mm × 4.4 mm    |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Schematic Symbol



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## 4 Revision History

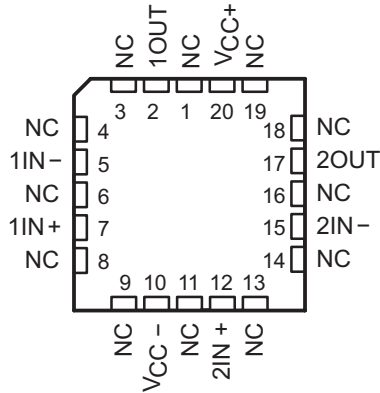
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision H (January 2014) to Revision I  | Page |
|---|------|
| • Added <i>Pin Configuration and Functions</i> section, <i>Storage Conditions</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | 1    |
| • Added <i>Applications</i> .....   | 1    |
| • Moved <i>Typical Characteristics</i> into <i>Specifications</i> section. ....   | 9    |

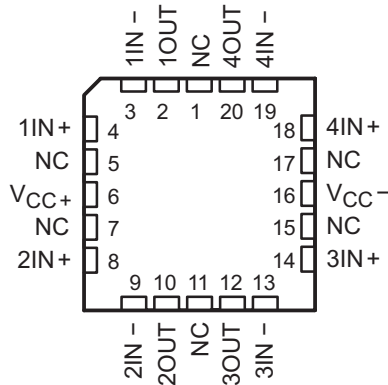
| Changes from Revision G (September 2004) to Revision H                          | Page |
|---|------|
| • Updated document to new TI data sheet format - no specification changes. .... | 1    |
| • Deleted <i>Ordering Information</i> table. ....                               | 1    |

## 5 Pin Configuration and Functions

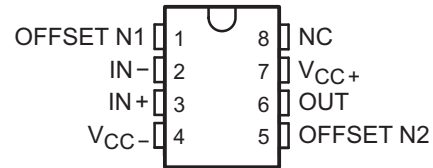
TL082 FK Package  
20-Pin LCCC  
Top View



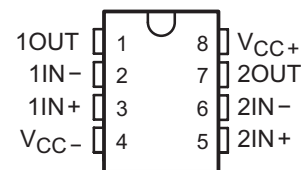
TL084 FK Package  
20-Pin LCCC  
Top View



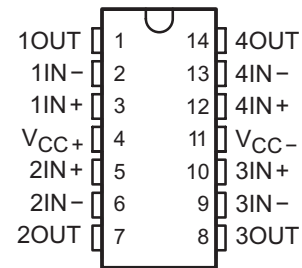
TL081 and TL081x D, P, and PS Package  
8-Pin SOIC, PDIP, and SO  
Top View



TL082 and TL082x D, JG, P, PS and PW Package  
8-Pin SOIC, CDIP, PDIP, SO, and TSSOP  
Top View



TL084 and TL084x D, J, N, NS and PW Package  
14-Pin SOIC, CDIP, PDIP, SO, and TSSOP  
Top View



### Pin Functions

| NAME | PIN            |                             |      |                             |      | I/O | DESCRIPTION    |
|------|----------------|-----------------------------|------|-----------------------------|------|-----|----------------|
|      | TL081          | TL082                       |      | TL084                       |      |     |                |
|      | SOIC, PDIP, SO | SOIC, CDIP, PDIP, SO, TSSOP | LCCC | SOIC, CDIP, PDIP, SO, TSSOP | LCCC |     |                |
| 1IN- | —              | 2                           | 5    | 2                           | 3    | I   | Negative input |
| 1IN+ | —              | 3                           | 7    | 3                           | 4    | I   | Positive input |
| 1OUT | —              | 1                           | 2    | 1                           | 2    | O   | Output         |
| 2IN- | —              | 6                           | 15   | 6                           | 9    | I   | Negative input |
| 2IN+ | —              | 5                           | 12   | 5                           | 8    | I   | Positive input |
| 2OUT | —              | 7                           | 17   | 7                           | 10   | O   | Output         |
| 3IN- | —              | —                           | —    | 9                           | 13   | I   | Negative input |
| 3IN+ | —              | —                           | —    | 10                          | 14   | I   | Positive input |
| 3OUT | —              | —                           | —    | 8                           | 12   | O   | Output         |
| 4IN- | —              | —                           | —    | 13                          | 19   | I   | Negative input |
| 4IN+ | —              | —                           | —    | 12                          | 18   | I   | Positive input |
| 4OUT | —              | —                           | —    | 14                          | 20   | O   | Output         |

Pin Functions (continued)

| NAME             | PIN            |                             |      |                             |      | I/O | DESCRIPTION             |
|------------------|----------------|-----------------------------|------|-----------------------------|------|-----|-------------------------|
|                  | TL081          | TL082                       |      | TL084                       |      |     |                         |
|                  | SOIC, PDIP, SO | SOIC, CDIP, PDIP, SO, TSSOP | LCCC | SOIC, CDIP, PDIP, SO, TSSOP | LCCC |     |                         |
| IN-              | 2              | —                           | —    | —                           | —    | I   | Negative input          |
| IN+              | 3              | —                           | —    | —                           | —    | I   | Positive input          |
| NC               | 8              | —                           | 1    | —                           | 1    | —   | Do not connect          |
|                  |                |                             | 3    |                             | 5    |     |                         |
|                  |                |                             | 4    |                             | 7    |     |                         |
|                  |                |                             | 6    |                             | 11   |     |                         |
|                  |                |                             | 8    |                             | 15   |     |                         |
|                  |                |                             | 9    |                             | 17   |     |                         |
|                  |                |                             | 11   |                             |      |     |                         |
|                  |                |                             | 13   |                             |      |     |                         |
|                  |                |                             | 14   |                             |      |     |                         |
|                  |                |                             | 16   |                             |      |     |                         |
| 18               |                |                             |      |                             |      |     |                         |
| OFFSET N1        | 1              | —                           | —    | —                           | —    | —   | Input offset adjustment |
| OFFSET N2        | 5              | —                           | —    | —                           | —    | —   | Input offset adjustment |
| OUT              | 6              | —                           | —    | —                           | —    | O   | Output                  |
| V <sub>CC-</sub> | 4              | 4                           | 10   | 11                          | 16   | —   | Power supply            |
| V <sub>CC+</sub> | 7              | 8                           | 20   | 4                           | 6    | —   | Power supply            |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |  |                              | MIN  | MAX | UNIT |
|-----------|--|------------------------------|--|-----|------|
| $V_{CC+}$ | Supply voltage <sup>(2)</sup>                                |                              |  | 18  | V    |
| $V_{CC-}$ |  |                              |  | -18 |      |
| $V_{ID}$  | Differential input voltage <sup>(3)</sup>                    |                              |  | ±30 | V    |
| $V_I$     | Input voltage <sup>(2)(4)</sup>                              |                              |  | ±15 | V    |
|           | Duration of output short circuit <sup>(5)</sup>              |                              | Unlimited                                    |     |      |
|           | Continuous total power dissipation                           |                              | See <a href="#">Dissipation Rating Table</a> |     |      |
| $T_A$     | Operating free-air temperature                               | TL08_C<br>TL08_AC<br>TL08_BC | 0  | 70  | °C   |
|           |  | TL08_I                       | -40  | 85  |      |
|           |  | TL084Q                       | -40  | 125 |      |
|           |  | TL08_M                       | -55  | 125 |      |
|           | Operating virtual junction temperature                       |                              |  | 150 | °C   |
| $T_C$     | Case temperature for 60 seconds                              | FK package                   | TL08_M                                       | 260 | °C   |
|           | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | J or JG package              | TL08_M                                       | 300 | °C   |
| $T_{stg}$ | Storage temperature  |                              | -65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
- (3) Differential voltages are at  $IN+$ , with respect to  $IN-$ .
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

### 6.2 ESD Ratings

|             |                         |  | VALUE | UNIT |
|-------------|-------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | 1000  | V    |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | 1500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|           |                     |        | MIN           | MAX           | UNIT |
|-----------|---------------------|--------|---------------|---------------|------|
| $V_{CC+}$ | Supply voltage      |        | 5             | 15            | V    |
| $V_{CC-}$ | Supply voltage      |        | -5            | -15           | V    |
| $V_{CM}$  | Common-mode voltage |        | $V_{CC-} + 4$ | $V_{CC+} - 4$ | V    |
| $T_A$     | Ambient temperature | TL08xM | -55           | 125           | °C   |
|           |                     | TL08xQ | -40           | 125           |      |
|           |                     | TL08xl | -40           | 85            |      |
|           |                     | TL08xC | 0             | 70            |      |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup>   | TL08xx   |         |          |         |                  |                  |            |         | UNIT |
|---|----------|---------|----------|---------|------------------|------------------|------------|---------|------|
|   | D (SOIC) |         | N (PDIP) | NS (SO) | P (PDIP)         | PS (SO)          | PW (TSSOP) |         |      |
|   | 8 PINS   | 14 PINS | 14 PINS  | 14 PINS | {PIN COUNT} PINS | {PIN COUNT} PINS | 8 PINS     | 14 PINS |      |
| R <sub>θJA</sub> Junction-to-ambient thermal resistance <sup>(2)(3)</sup> | 97       | 86      | 76       | 80      | 85               | 95               | 149        | 113     | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>) / R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI

V<sub>CC±</sub> = ±15 V (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS   | T <sub>A</sub> <sup>(1)</sup> | TL081C, TL082C, TL084C |                  |     | TL081AC, TL082AC, TL084AC |                  |     | TL081BC, TL082BC, TL084BC |                  |     | TL081I, TL082I, TL084I |                  |      | UNIT  |
|--|---|-------------------------------|------------------------|------------------|-----|---------------------------|------------------|-----|---------------------------|------------------|-----|------------------------|------------------|------|-------|
|  |   |                               | MIN                    | TYP              | MAX | MIN                       | TYP              | MAX | MIN                       | TYP              | MAX | MIN                    | TYP              | MAX  |       |
| V <sub>IO</sub> Input offset voltage   | V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω   | 25°C                          |                        | 3                | 15  |                           | 3                | 6   |                           | 2                | 3   |                        | 3                | 6    | mV    |
|  |   | Full range                    |                        |                  | 20  |                           |                  | 7.5 |                           |                  | 5   |                        |                  | 9    |       |
| α <sub>VIO</sub> Temperature coefficient of input offset voltage                       | V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω   | Full range                    |                        | 18               |     |                           | 18               |     |                           | 18               |     |                        | 18               |      | μV/°C |
| I <sub>IO</sub> Input offset current <sup>(2)</sup>                                    | V <sub>O</sub> = 0  | 25°C                          |                        | 5                | 200 |                           | 5                | 100 |                           | 5                | 100 |                        | 5                | 100  | pA    |
|  |   | Full range                    |                        |                  | 2   |                           |                  | 2   |                           |                  | 2   |                        |                  | 10   | nA    |
| I <sub>IB</sub> Input bias current <sup>(2)</sup>                                      | V <sub>O</sub> = 0  | 25°C                          |                        | 30               | 400 |                           | 30               | 200 |                           | 30               | 200 |                        | 30               | 200  | pA    |
|  |   | Full range                    |                        |                  | 10  |                           |                  | 7   |                           |                  | 7   |                        |                  | 20   | nA    |
| V <sub>ICR</sub> Common-mode input voltage range                                       |   | 25°C                          | ±11                    | -12 to 15        |     | ±11                       | -12 to 15        |     | ±11                       | -12 to 15        |     | ±11                    | -12 to 15        | V    |       |
| V <sub>OM</sub> Maximum peak output voltage swing                                      | R <sub>L</sub> = 10 kΩ  | 25°C                          | ±12                    | ±13.5            |     | ±12                       | ±13.5            |     | ±12                       | ±13.5            |     | ±12                    | ±13.5            | V    |       |
|  | R <sub>L</sub> ≥ 10 kΩ  |                               | ±12                    |                  |     | ±12                       |                  |     | ±12                       |                  |     | ±12                    |                  |      |       |
|  | R <sub>L</sub> ≥ 2 kΩ   | Full range                    | ±10                    | ±12              |     | ±10                       | ±12              |     | ±10                       | ±12              |     | ±10                    | ±12              |      |       |
| A <sub>VD</sub> Large-signal differential voltage amplification                        | V <sub>O</sub> = ±10 V, R <sub>L</sub> ≥ 2 kΩ                                     | 25°C                          | 25                     | 200              |     | 50                        | 200              |     | 50                        | 200              |     | 50                     | 200              | V/mV |       |
|  |   | Full range                    | 15                     |                  |     | 15                        |                  |     | 25                        |                  |     | 25                     |                  |      |       |
| B <sub>1</sub> Unity-gain bandwidth  |   | 25°C                          |                        | 3                |     |                           | 3                |     |                           | 3                |     |                        | 3                | MHz  |       |
| r <sub>i</sub> Input resistance  |   | 25°C                          |                        | 10 <sup>12</sup> |     |                           | 10 <sup>12</sup> |     |                           | 10 <sup>12</sup> |     |                        | 10 <sup>12</sup> | Ω    |       |
| CMRR Common-mode rejection ratio   | V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω | 25°C                          | 70                     | 86               |     | 75                        | 86               |     | 75                        | 86               |     | 75                     | 86               | dB   |       |
| k <sub>SVR</sub> Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> ) | V <sub>CC</sub> = ±15 V to ±9 V, V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω        | 25°C                          | 70                     | 86               |     | 80                        | 86               |     | 80                        | 86               |     | 80                     | 86               | dB   |       |

- (1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T<sub>A</sub> is 0°C to 70°C for TL08\_C, TL08\_AC, TL08\_BC and –40°C to 85°C for TL08\_I.
- (2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 13](#). Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

## Electrical Characteristics for TL08xC, TL08xxC, and TL08xl (continued)

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS                 | $T_A^{(1)}$         | TL081C, TL082C, TL084C |     |     | TL081AC, TL082AC, TL084AC |     |     | TL081BC, TL082BC, TL084BC |     |     | TL081I, TL082I, TL084I |     |     | UNIT |
|-----------------|---------------------------------|---------------------|------------------------|-----|-----|---------------------------|-----|-----|---------------------------|-----|-----|------------------------|-----|-----|------|
|                 |                                 |                     | MIN                    | TYP | MAX | MIN                       | TYP | MAX | MIN                       | TYP | MAX | MIN                    | TYP | MAX |      |
| $I_{CC}$        | Supply current (each amplifier) | $V_O = 0$ , No load | 25°C                   | 1.4 | 2.8 | 1.4                       | 2.8 | 1.4 | 2.8                       | 1.4 | 2.8 | 1.4                    | 2.8 | mA  |      |
| $V_{O1}/V_{O2}$ | Crosstalk attenuation           | $A_{VD} = 100$      | 25°C                   | 120 |     | 120                       |     | 120 |                           | 120 |     | 120                    |     | dB  |      |

## 6.6 Electrical Characteristics for TL08xM and TL084x

 $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS <sup>(1)</sup>                                      | $T_A$   | TL081M, TL082M |           |            | TL084Q, TL084M |            |                              | UNIT |
|-----------------|---|---|----------------|-----------|------------|----------------|------------|------------------------------|------|
|                 |   |   | MIN            | TYP       | MAX        | MIN            | TYP        | MAX                          |      |
| $V_{IO}$        | Input offset voltage  | $V_O = 0$ , $R_S = 50\ \Omega$  | 25°C           | 3         | 6          | 3              | 9          | mV                           |      |
|                 |   |   | Full range     |           | 9          |                | 15         |                              |      |
| $\alpha_{VIO}$  | Temperature coefficient of input offset voltage                     | $V_O = 0$ , $R_S = 50\ \Omega$  | Full range     | 18        |            | 18             |            | $\mu\text{V}/^\circ\text{C}$ |      |
| $I_{IO}$        | Input offset current <sup>(2)</sup>                                 | $V_O = 0$   | 25°C           | 5         | 100        | 5              | 100        | pA                           |      |
|                 |   |   | 125°C          |           | 20         |                | 20         |                              |      |
| $I_{IB}$        | Input bias current <sup>(2)</sup>                                   | $V_O = 0$   | 25°C           | 30        | 200        | 30             | 200        | pA                           |      |
|                 |   |   | 125°C          |           | 50         |                | 50         |                              |      |
| $V_{ICR}$       | Common-mode input voltage range                                     |   | 25°C           | $\pm 11$  | -12 to 15  | $\pm 11$       | -12 to 15  | V                            |      |
| $V_{OM}$        | Maximum peak output voltage swing                                   | $R_L = 10\ \text{k}\Omega$  | 25°C           | $\pm 12$  | $\pm 13.5$ | $\pm 12$       | $\pm 13.5$ | V                            |      |
|                 |   | $R_L \geq 10\ \text{k}\Omega$   | Full range     | $\pm 12$  |            | $\pm 12$       |            |                              |      |
|                 |   | $R_L \geq 2\ \text{k}\Omega$  |                | $\pm 10$  | $\pm 12$   | $\pm 10$       | $\pm 12$   |                              |      |
| $A_{VD}$        | Large-signal differential voltage amplification                     | $V_O = \pm 10\ \text{V}$ , $R_L \geq 2\ \text{k}\Omega$                           | 25°C           | 25        | 200        | 25             | 200        | V/mV                         |      |
|                 |   |   | Full range     | 15        |            | 15             |            |                              |      |
| $B_1$           | Unity-gain bandwidth  |   | 25°C           | 3         |            | 3              |            | MHz                          |      |
| $r_i$           | Input resistance  |   | 25°C           | $10^{12}$ |            | $10^{12}$      |            | $\Omega$                     |      |
| CMRR            | Common-mode rejection ratio   | $V_{IC} = V_{ICRmin}$ , $V_O = 0$ , $R_S = 50\ \Omega$                            | 25°C           | 80        | 86         | 80             | 86         | dB                           |      |
| $k_{SVR}$       | Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ ) | $V_{CC} = \pm 15\ \text{V}$ to $\pm 9\ \text{V}$ , $V_O = 0$ , $R_S = 50\ \Omega$ | 25°C           | 80        | 86         | 80             | 86         | dB                           |      |
| $I_{CC}$        | Supply current (each amplifier)                                     | $V_O = 0$ , No load   | 25°C           | 1.4       | 2.8        | 1.4            | 2.8        | mA                           |      |
| $V_{O1}/V_{O2}$ | Crosstalk attenuation   | $A_{VD} = 100$  | 25°C           | 120       |            | 120            |            | dB                           |      |

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

## 6.7 Operating Characteristics

 $V_{CC\pm} = \pm 15\ \text{V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER | TEST CONDITIONS  | MIN              | TYP | MAX | UNIT             |
|-----------|--|------------------|-----|-----|------------------|
| SR        | $V_I = 10\ \text{V}$ , $R_L = 2\ \text{k}\Omega$ , $C_L = 100\ \text{pF}$ ,<br>See Figure 19   | 8 <sup>(1)</sup> | 13  |     | V/ $\mu\text{s}$ |
|           | $V_I = 10\ \text{V}$ , $R_L = 2\ \text{k}\Omega$ , $C_L = 100\ \text{pF}$ ,<br>$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ ,<br>See Figure 19 | 5 <sup>(1)</sup> |     |     |                  |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## Operating Characteristics (continued)

$V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER |                                | TEST CONDITIONS   |                                      | MIN | TYP    | MAX | UNIT                         |
|-----------|--------------------------------|---|--------------------------------------|-----|--------|-----|------------------------------|
| $t_r$     | Rise-time                      | $V_I = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ ,<br>See <a href="#">Figure 19</a>                                 |                                      |     | 0.05   |     | $\mu\text{s}$                |
|           | overshoot factor               |   |                                      |     | 20%    |     |                              |
| $V_n$     | Equivalent input noise voltage | $R_S = 20\ \Omega$  | $f = 1\text{ kHz}$                   |     | 18     |     | $\text{nV}/\sqrt{\text{Hz}}$ |
|           |                                |   | $f = 10\text{ Hz to } 10\text{ kHz}$ |     | 4      |     | $\mu\text{V}$                |
| $I_n$     | Equivalent input noise current | $R_S = 20\ \Omega$ ,  | $f = 1\text{ kHz}$                   |     | 0.01   |     | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD       | Total harmonic distortion      | $V_{\text{rms}} = 6\text{ V}$ , $A_{\text{VD}} = 1$ , $R_S \leq 1\text{ k}\Omega$ , $R_L \geq 2\text{ k}\Omega$ ,<br>$f = 1\text{ kHz}$ , |                                      |     | 0.003% |     |                              |

## 6.8 Dissipation Rating Table

| PACKAGE    | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING<br>FACTOR        | DERATE<br>ABOVE $T_A$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>POWER RATING | $T_A = 125^\circ\text{C}$<br>POWER RATING |
|------------|---|---------------------------|-----------------------|--|--|---|
| D (14 pin) | 680 mW                                      | 7.6 mW/ $^\circ\text{C}$  | 60 $^\circ\text{C}$   | 604 mW                                   | 490 mW                                   | 186 mW                                    |
| FK         | 680 mW                                      | 11.0 mW/ $^\circ\text{C}$ | 88 $^\circ\text{C}$   | 680 mW                                   | 680 mW                                   | 273 mW                                    |
| J          | 680 mW                                      | 11.0 mW/ $^\circ\text{C}$ | 88 $^\circ\text{C}$   | 680 mW                                   | 680 mW                                   | 273 mW                                    |
| JG         | 680 mW                                      | 8.4 mW/ $^\circ\text{C}$  | 69 $^\circ\text{C}$   | 672 mW                                   | 546 mW                                   | 210 mW                                    |

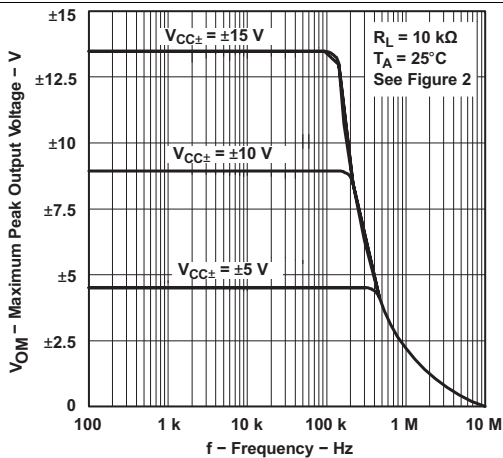


### 6.9 Typical Characteristics

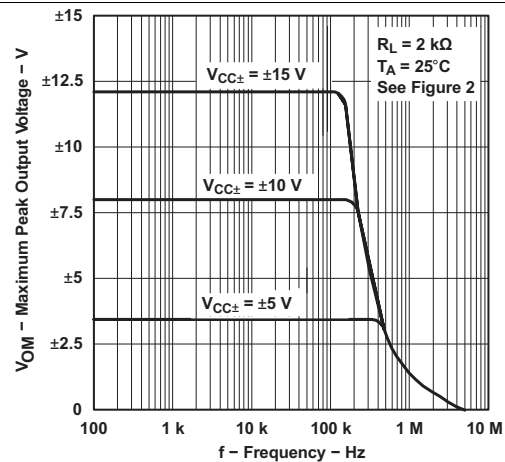
Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in [Parameter Measurement Information](#).

**Table 1. Table of Graphs**

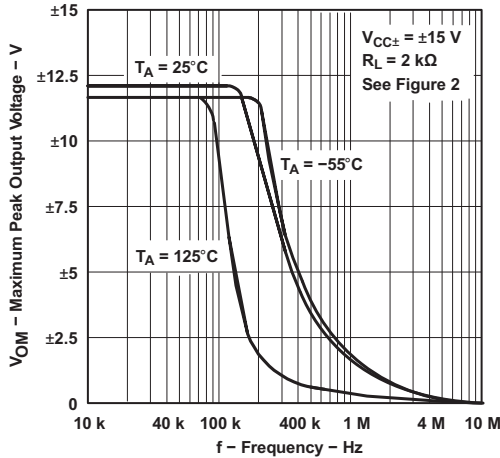
|          |   | Figure                       |
|----------|---|------------------------------|
| $V_{OM}$ | Maximum peak output voltage                     | Figure 1, Figure 2, Figure 3 |
|          |   | Figure 4                     |
|          |   | Figure 5                     |
|          |   | Figure 6                     |
| $A_{VD}$ | Large-signal differential voltage amplification | Figure 7<br>Figure 8         |
|          | Differential voltage amplification              | Figure 9                     |
| $P_D$    | Total power dissipation                         | Figure 10                    |
| $I_{CC}$ | Supply current                                  | Figure 11                    |
|          |   | Figure 12                    |
| $I_{IB}$ | Input bias current                              | Figure 13                    |
|          | Large-signal pulse response                     | Figure 14                    |
| $V_O$    | Output voltage                                  | Figure 15                    |
| CMRR     | Common-mode rejection ratio                     | Figure 16                    |
| $V_n$    | Equivalent input noise voltage                  | Figure 17                    |
| THD      | Total harmonic distortion                       | Figure 18                    |



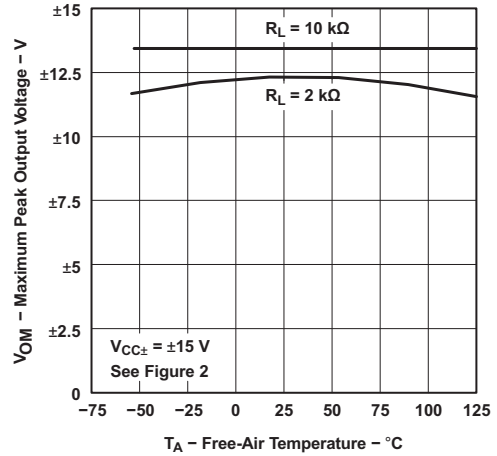
**Figure 1. Maximum Peak Output Voltage vs Frequency**



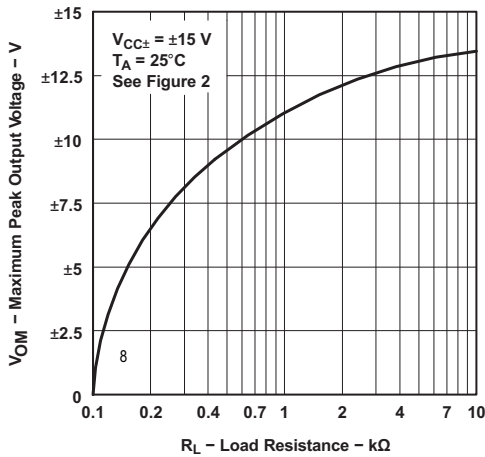
**Figure 2. Maximum Peak Output Voltage vs Frequency**



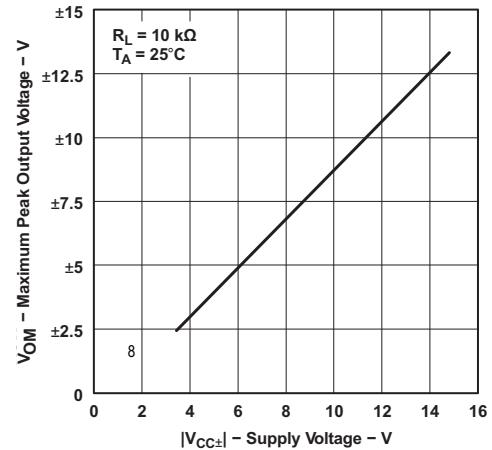
**Figure 3. Maximum Peak Output Voltage vs Frequency**



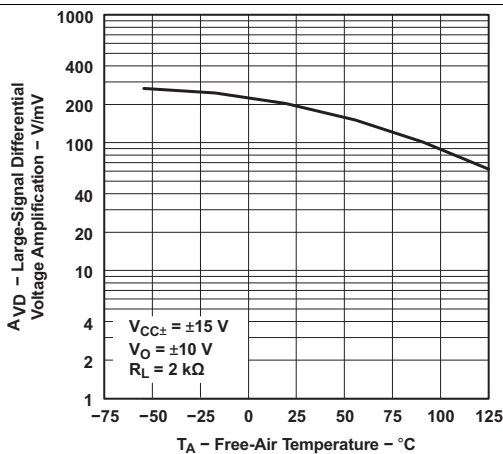
**Figure 4. Maximum Peak Output Voltage vs Free-Air Temperature**



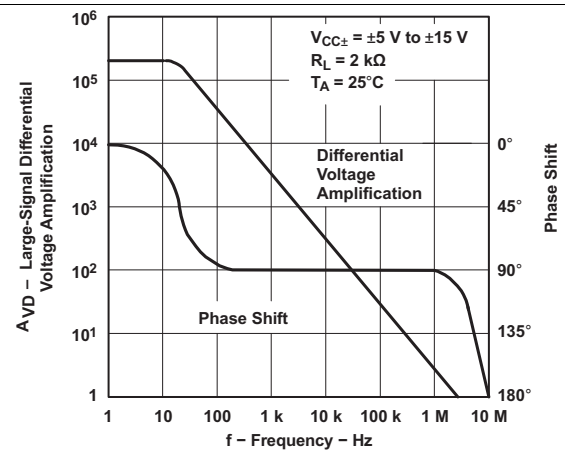
**Figure 5. Maximum Peak Output Voltage vs Load Resistance**



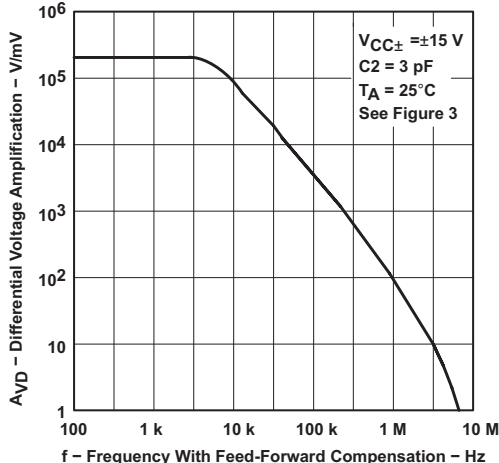
**Figure 6. Maximum Peak Output Voltage vs Supply Voltage**



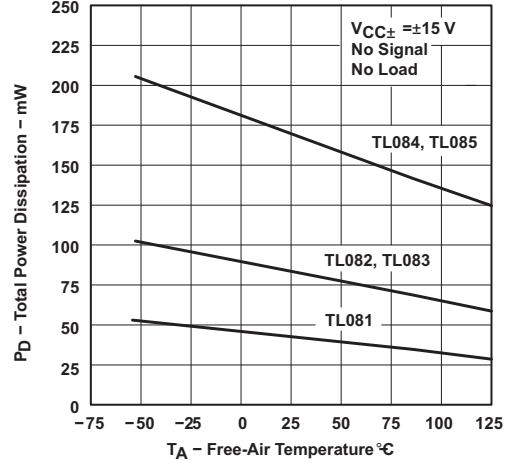
**Figure 7. Large-Signal Differential Voltage Amplification vs Free-Air Temperature**



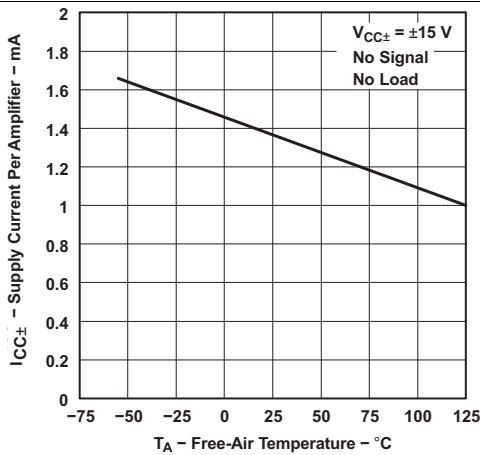
**Figure 8. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency**



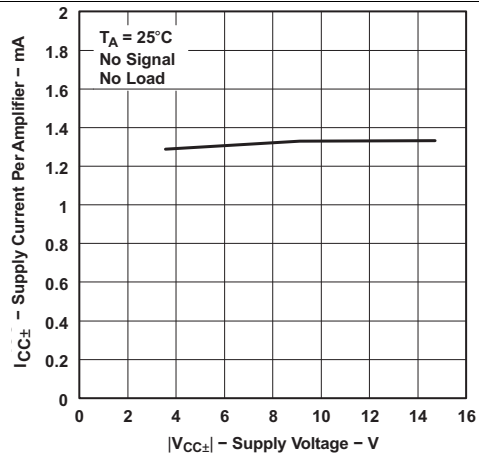
**Figure 9. Differential Voltage Amplification vs Frequency with Feed-Forward Compensation**



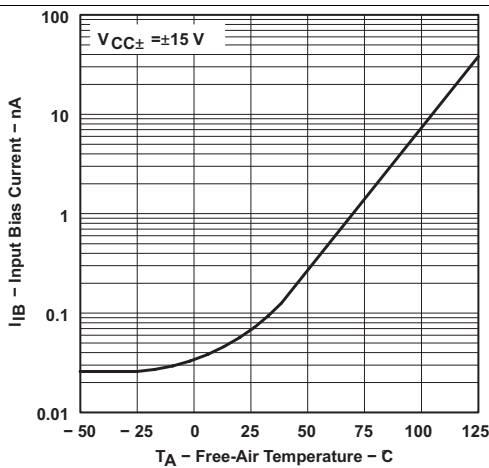
**Figure 10. Total Power Dissipation vs Free-Air Temperature**



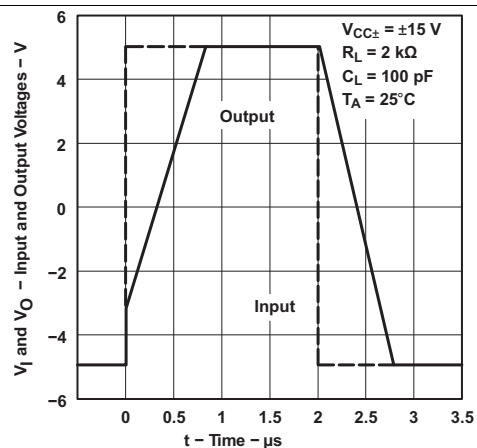
**Figure 11. Supply Current per Amplifier vs Free-Air Temperature**



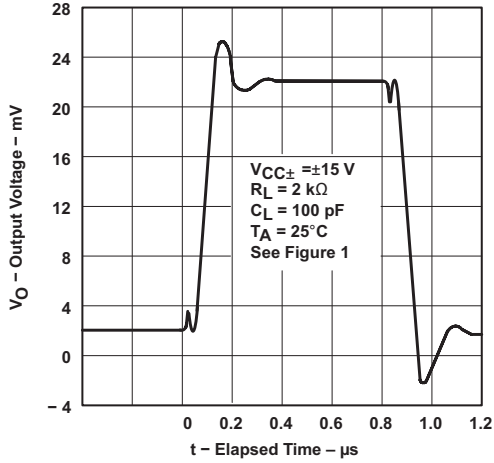
**Figure 12. Supply Current per Amplifier vs Supply Voltage**



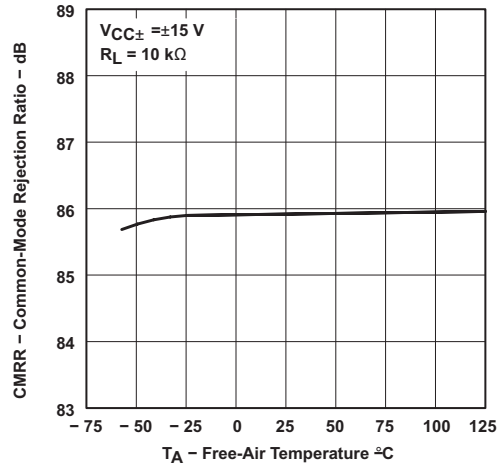
**Figure 13. Input Bias Current vs Free-Air Temperature**



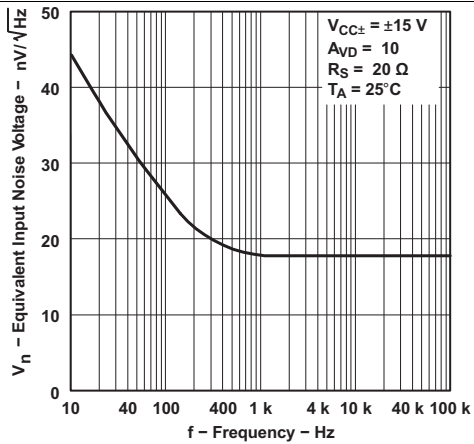
**Figure 14. Voltage-Follower Large-Signal Pulse Response**



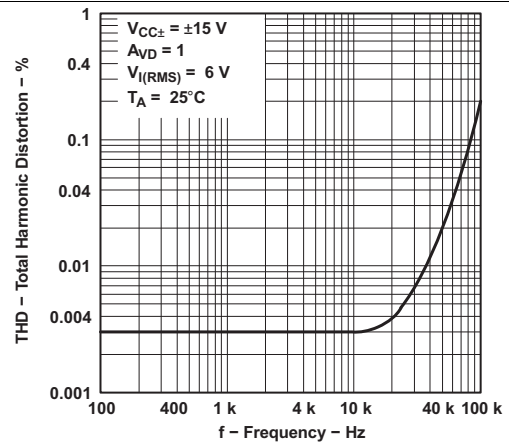
**Figure 15. Output Voltage vs Elapsed Time**



**Figure 16. Common-Mode Rejection Ratio vs Free-Air Temperature**



**Figure 17. Equivalent Input Noise Voltage vs Frequency**



**Figure 18. Total Harmonic Distortion vs Frequency**

## 7 Parameter Measurement Information

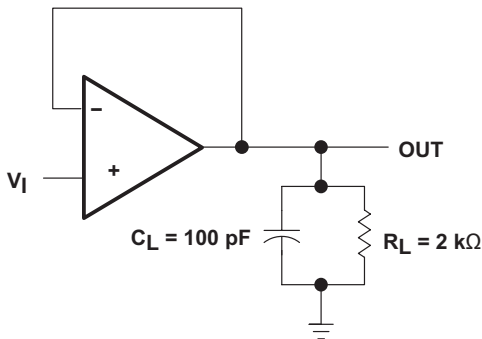


Figure 19. Test Figure 1

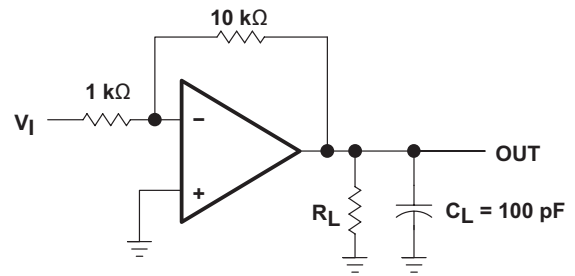


Figure 20. Test Figure 2

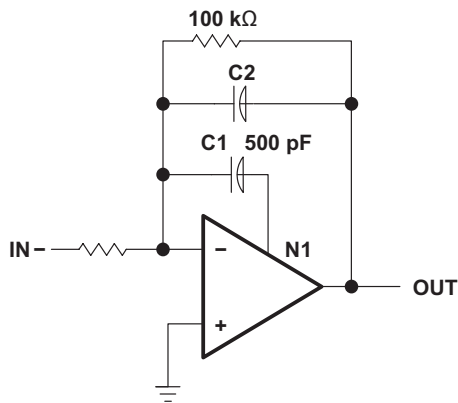


Figure 21. Test Figure 3

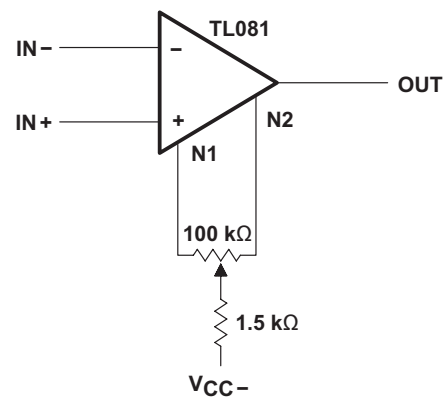


Figure 22. Test Figure 4

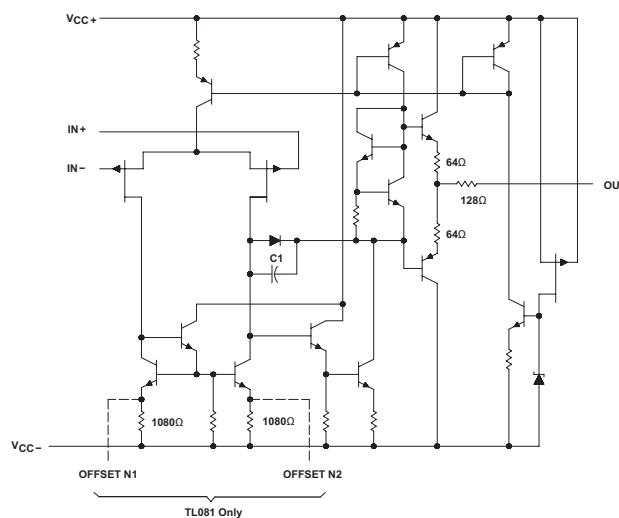
## 8 Detailed Description

### 8.1 Overview

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08xx family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The Q-suffix devices are characterized for operation from -40°C to +125°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to +125°C.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices will add little harmonic distortion when used in audio signal applications.

#### 8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/μs slew rate.

### 8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

## 9 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

### 9.2 Typical Applications

#### 9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

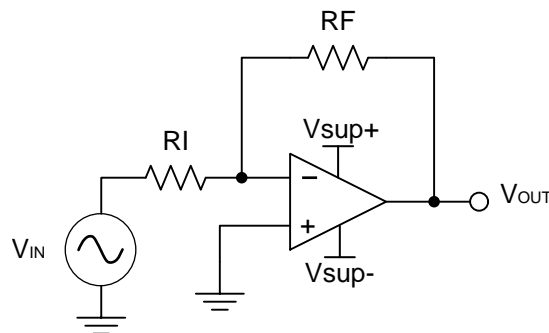


Figure 23. Schematic for Inverting Amplifier Application

##### 9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

##### 9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . Choosing a value in the  $k\Omega$  range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose  $10$   $k\Omega$  for  $R_I$  which means  $36$   $k\Omega$  will be used for  $R_F$ . This was determined by Equation 3.

$$A_v = -\frac{R_F}{R_I} \quad (3)$$

## Typical Applications (continued)

### 9.2.1.3 Application Curve

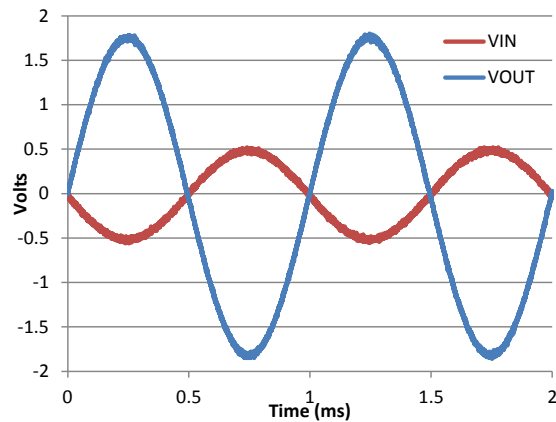


Figure 24. Input and output voltages of the inverting amplifier

## 9.3 System Examples

### 9.3.1 General Applications

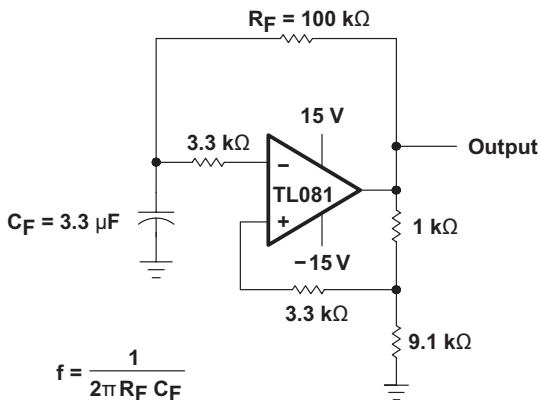


Figure 25. 0.5-Hz Square-Wave Oscillator

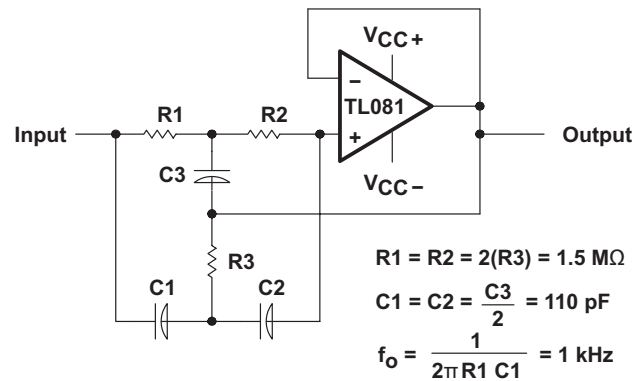


Figure 26. High-Q Notch Filter

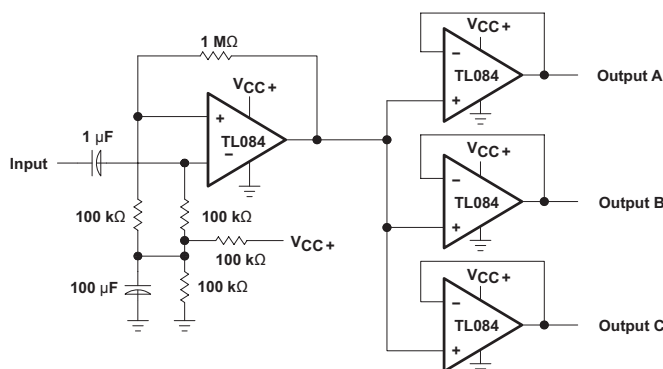


Figure 27. Audio-Distribution Amplifier

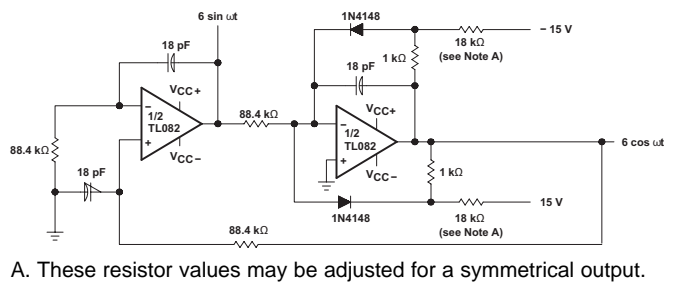
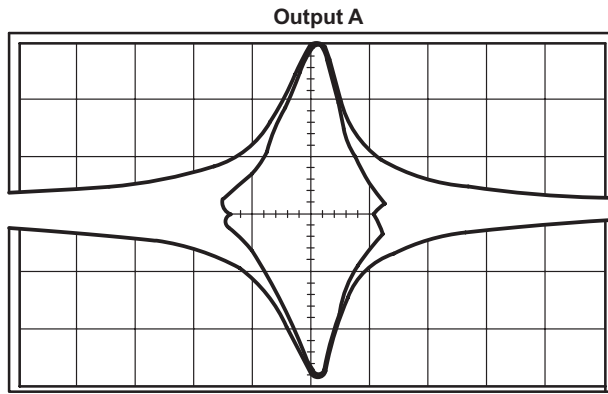
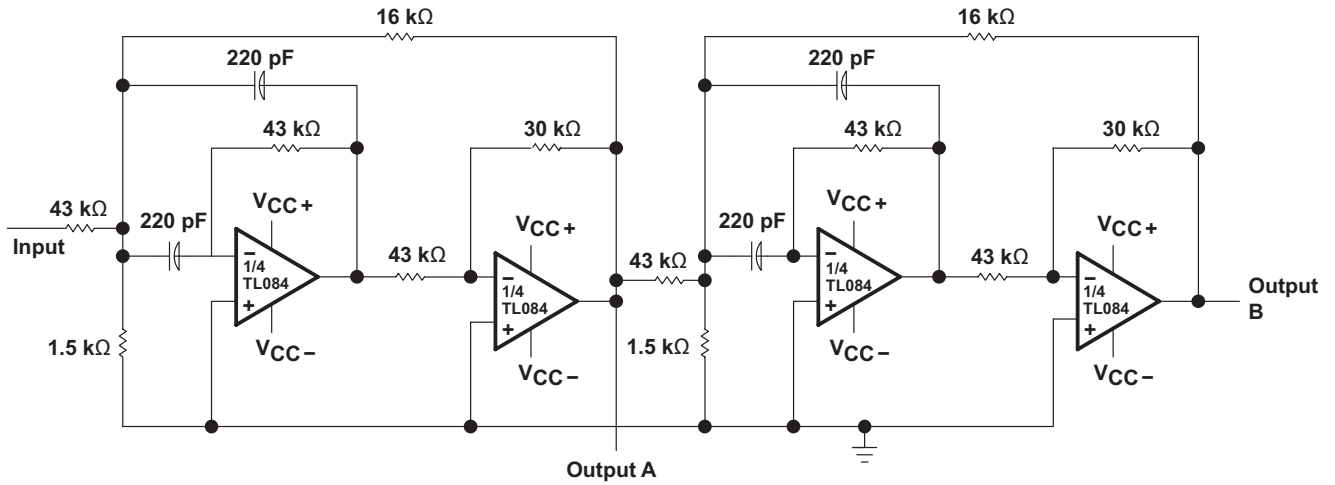


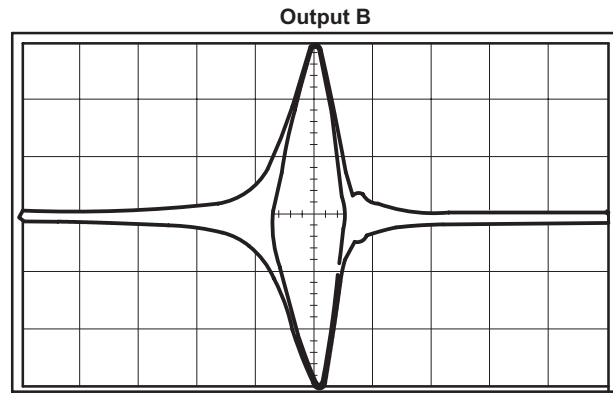
Figure 28. 100-kHz Quadrature Oscillator



System Examples (continued)



2 kHz/div  
Second-Order Bandpass Filter  
 $f_o = 100$  kHz,  $Q = 30$ , GAIN = 4



2 kHz/div  
Cascaded Bandpass Filter  
 $f_o = 100$  kHz,  $Q = 69$ , GAIN = 16

Figure 29. Positive-Feedback Bandpass Filter

## 10 Power Supply Recommendations

### CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of  $\pm 18$  V for a dual-supply can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#).

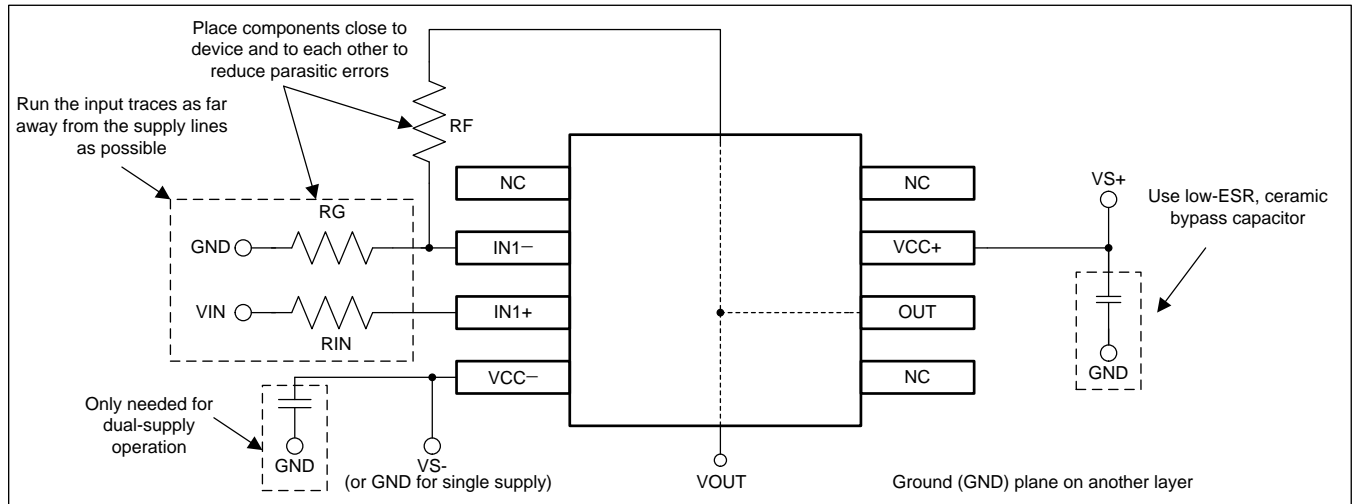
## 11 Layout

### 11.1 Layout Guidelines

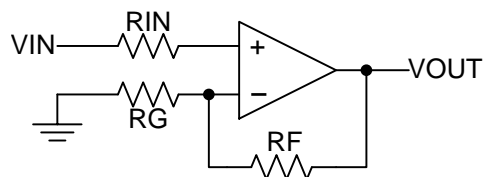
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to [Circuit Board Layout Techniques](#), (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Examples](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Examples



**Figure 30. Operational Amplifier Board Layout for Noninverting Configuration**



**Figure 31. Operational Amplifier Schematic for Noninverting Configuration**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For more information, see the following:

- *Circuit Board Layout Techniques*, [SLOA089](#).

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS  | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|--------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TL081  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL081A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL081B | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL082  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL082A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL082B | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL084  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL084A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TL084B | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
 All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)              | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|--------------------------------------|-------------------------|
| 5962-9851501Q2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9851501Q2A<br>TL082MFKB     | <a href="#">Samples</a> |
| 5962-9851501QPA  | ACTIVE        | CDIP         | JG                 | 8    | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 9851501QPA<br>TL082M                 | <a href="#">Samples</a> |
| 5962-9851503Q2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9851503Q2A<br>TL084<br>MFKB | <a href="#">Samples</a> |
| 5962-9851503QCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9851503QC<br>A<br>TL084MJB      | <a href="#">Samples</a> |
| TL081ACD         | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 081AC                                | <a href="#">Samples</a> |
| TL081ACDR        | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 081AC                                | <a href="#">Samples</a> |
| TL081ACP         | ACTIVE        | PDIP         | P                  | 8    | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL081ACP                             | <a href="#">Samples</a> |
| TL081BCD         | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 081BC                                | <a href="#">Samples</a> |
| TL081BCDR        | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 081BC                                | <a href="#">Samples</a> |
| TL081BCP         | ACTIVE        | PDIP         | P                  | 8    | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL081BCP                             | <a href="#">Samples</a> |
| TL081BCPE4       | ACTIVE        | PDIP         | P                  | 8    | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL081BCP                             | <a href="#">Samples</a> |
| TL081CD          | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL081C                               | <a href="#">Samples</a> |
| TL081CDR         | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL081C                               | <a href="#">Samples</a> |
| TL081CP          | ACTIVE        | PDIP         | P                  | 8    | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL081CP                              | <a href="#">Samples</a> |
| TL081CPE4        | ACTIVE        | PDIP         | P                  | 8    | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL081CP                              | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL081CPSR        | ACTIVE        | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T081                    | <a href="#">Samples</a> |
| TL081ID          | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL081I                  | <a href="#">Samples</a> |
| TL081IDR         | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL081I                  | <a href="#">Samples</a> |
| TL081IP          | ACTIVE        | PDIP         | P               | 8    | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | TL081IP                 | <a href="#">Samples</a> |
| TL082ACD         | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082AC                   | <a href="#">Samples</a> |
| TL082ACDE4       | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082AC                   | <a href="#">Samples</a> |
| TL082ACDG4       | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082AC                   | <a href="#">Samples</a> |
| TL082ACDR        | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082AC                   | <a href="#">Samples</a> |
| TL082ACDRE4      | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082AC                   | <a href="#">Samples</a> |
| TL082ACDRG4      | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082AC                   | <a href="#">Samples</a> |
| TL082ACP         | ACTIVE        | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL082ACP                | <a href="#">Samples</a> |
| TL082ACPSR       | ACTIVE        | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T082A                   | <a href="#">Samples</a> |
| TL082BCD         | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082BC                   | <a href="#">Samples</a> |
| TL082BCDE4       | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082BC                   | <a href="#">Samples</a> |
| TL082BCDR        | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082BC                   | <a href="#">Samples</a> |
| TL082BCDRE4      | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082BC                   | <a href="#">Samples</a> |
| TL082BCDRG4      | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | 082BC                   | <a href="#">Samples</a> |
| TL082BCP         | ACTIVE        | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL082BCP                | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL082BCPE4       | ACTIVE        | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL082BCP                | <a href="#">Samples</a> |
| TL082CD          | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL082C                  | <a href="#">Samples</a> |
| TL082CDE4        | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL082C                  | <a href="#">Samples</a> |
| TL082CDR         | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL082C                  | <a href="#">Samples</a> |
| TL082CDRE4       | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL082C                  | <a href="#">Samples</a> |
| TL082CDRG4       | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL082C                  | <a href="#">Samples</a> |
| TL082CP          | ACTIVE        | PDIP         | P               | 8    | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL082CP                 | <a href="#">Samples</a> |
| TL082CPSR        | ACTIVE        | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T082                    | <a href="#">Samples</a> |
| TL082CPSRG4      | ACTIVE        | SO           | PS              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T082                    | <a href="#">Samples</a> |
| TL082CPW         | ACTIVE        | TSSOP        | PW              | 8    | 150         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T082                    | <a href="#">Samples</a> |
| TL082CPWR        | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T082                    | <a href="#">Samples</a> |
| TL082CPWRG4      | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T082                    | <a href="#">Samples</a> |
| TL082ID          | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL082I                  | <a href="#">Samples</a> |
| TL082IDG4        | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL082I                  | <a href="#">Samples</a> |
| TL082IDR         | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL082I                  | <a href="#">Samples</a> |
| TL082IDRE4       | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL082I                  | <a href="#">Samples</a> |
| TL082IDRG4       | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL082I                  | <a href="#">Samples</a> |
| TL082IP          | ACTIVE        | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | TL082IP                 | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)      | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|------------------------------|-------------------------|
| TL082IPE4        | ACTIVE        | PDIP         | P               | 8    | 50          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | TL082IP                      | <a href="#">Samples</a> |
| TL082IPWR        | ACTIVE        | TSSOP        | PW              | 8    | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | Z082                         | <a href="#">Samples</a> |
| TL082MFKB        | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-9851501Q2A<br>TL082MFKB | <a href="#">Samples</a> |
| TL082MJG         | ACTIVE        | CDIP         | JG              | 8    | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | TL082MJG                     | <a href="#">Samples</a> |
| TL082MJGB        | ACTIVE        | CDIP         | JG              | 8    | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 9851501QPA<br>TL082M         | <a href="#">Samples</a> |
| TL084ACD         | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084AC                      | <a href="#">Samples</a> |
| TL084ACDE4       | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084AC                      | <a href="#">Samples</a> |
| TL084ACDR        | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084AC                      | <a href="#">Samples</a> |
| TL084ACDRE4      | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084AC                      | <a href="#">Samples</a> |
| TL084ACDRG4      | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084AC                      | <a href="#">Samples</a> |
| TL084ACN         | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL084ACN                     | <a href="#">Samples</a> |
| TL084ACNSR       | ACTIVE        | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084A                       | <a href="#">Samples</a> |
| TL084BCD         | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084BC                      | <a href="#">Samples</a> |
| TL084BCDR        | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084BC                      | <a href="#">Samples</a> |
| TL084BCDRG4      | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084BC                      | <a href="#">Samples</a> |
| TL084BCN         | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL084BCN                     | <a href="#">Samples</a> |
| TL084BCNE4       | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL084BCN                     | <a href="#">Samples</a> |
| TL084CD          | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084C                       | <a href="#">Samples</a> |



| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL084CDE4        | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084C                  | <a href="#">Samples</a> |
| TL084CDG4        | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084C                  | <a href="#">Samples</a> |
| TL084CDR         | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084C                  | <a href="#">Samples</a> |
| TL084CDRE4       | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084C                  | <a href="#">Samples</a> |
| TL084CDRG4       | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084C                  | <a href="#">Samples</a> |
| TL084CN          | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL084CN                 | <a href="#">Samples</a> |
| TL084CNE4        | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | TL084CN                 | <a href="#">Samples</a> |
| TL084CNSR        | ACTIVE        | SO           | NS              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | TL084                   | <a href="#">Samples</a> |
| TL084CPW         | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T084                    | <a href="#">Samples</a> |
| TL084CPWE4       | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T084                    | <a href="#">Samples</a> |
| TL084CPWR        | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | T084                    | <a href="#">Samples</a> |
| TL084ID          | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL084I                  | <a href="#">Samples</a> |
| TL084IDR         | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL084I                  | <a href="#">Samples</a> |
| TL084IDRE4       | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL084I                  | <a href="#">Samples</a> |
| TL084IDRG4       | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | TL084I                  | <a href="#">Samples</a> |
| TL084IN          | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | TL084IN                 | <a href="#">Samples</a> |
| TL084INE4        | ACTIVE        | PDIP         | N               | 14   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | TL084IN                 | <a href="#">Samples</a> |
| TL084MFK         | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | TL084MFK                | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)          | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|----------------------------------|-------------------------|
| TL084MFKB        | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-9851503Q2A<br>TL084<br>MFKB | <a href="#">Samples</a> |
| TL084MJ          | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | TL084MJ                          | <a href="#">Samples</a> |
| TL084MJB         | ACTIVE        | CDIP         | J               | 14   | 1           | TBD                     | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9851503QC<br>A<br>TL084MJB  | <a href="#">Samples</a> |
| TL084QD          | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TL084Q                           | <a href="#">Samples</a> |
| TL084QDG4        | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TL084Q                           | <a href="#">Samples</a> |
| TL084QDR         | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TL084Q                           | <a href="#">Samples</a> |
| TL084QDRG4       | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | TL084Q                           | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :**

- Catalog: [TL082](#), [TL084](#)
- Automotive: [TL082-Q1](#), [TL082-Q1](#)
- Military: [TL082M](#), [TL084M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

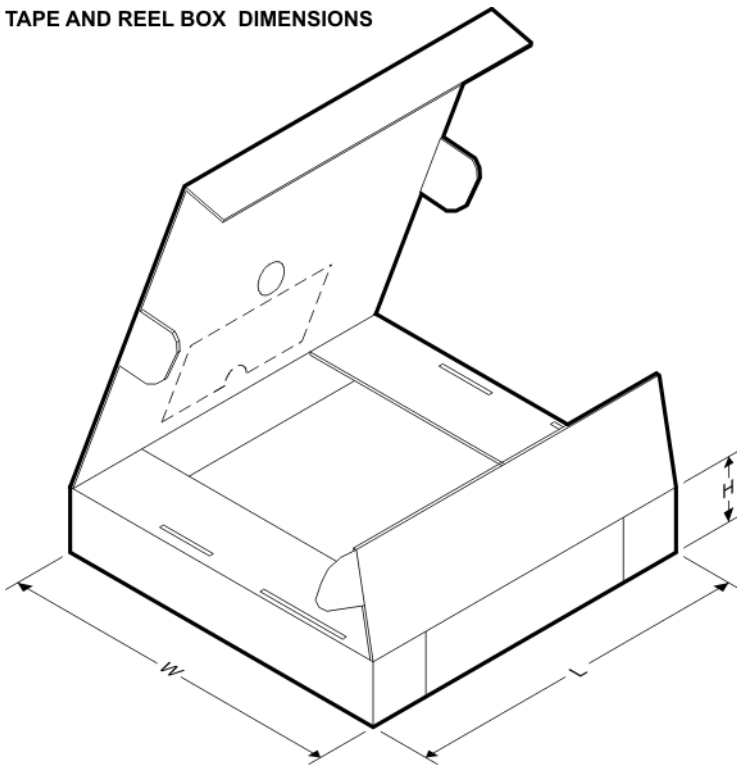
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL081ACDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL081BCDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL081CDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL081IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082ACDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082ACDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082BCDR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082CDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082CDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082CPWR  | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TL082IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL082IPWR  | TSSOP        | PW              | 8    | 2000 | 330.0              | 12.4               | 7.0     | 3.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TL084ACDR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL084ACDR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL084ACNSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| TL084BCDR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL084CDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL084CDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL084CDRG4 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL084CPWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TL084IDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL084QDR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TL084QDRG4 | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL081ACDR | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL081BCDR | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL081CDR  | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL081IDR  | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL082ACDR | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL082ACDR | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| TL082BCDR | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL082CDR  | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| TL082CDR  | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL082CPWR | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |
| TL082IDR  | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL082IDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| TL082IPWR  | TSSOP        | PW              | 8    | 2000 | 367.0       | 367.0      | 35.0        |
| TL084ACDR  | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| TL084ACDR  | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| TL084ACNSR | SO           | NS              | 14   | 2000 | 367.0       | 367.0      | 38.0        |
| TL084BCDR  | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| TL084CDR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| TL084CDR   | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| TL084CDRG4 | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| TL084CPWR  | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| TL084IDR   | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| TL084QDR   | SOIC         | D               | 14   | 2500 | 350.0       | 350.0      | 43.0        |
| TL084QDRG4 | SOIC         | D               | 14   | 2500 | 350.0       | 350.0      | 43.0        |

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

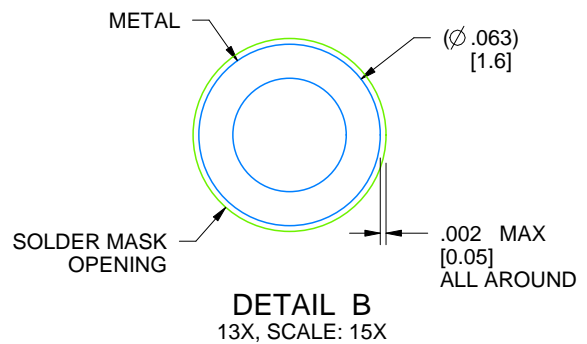
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

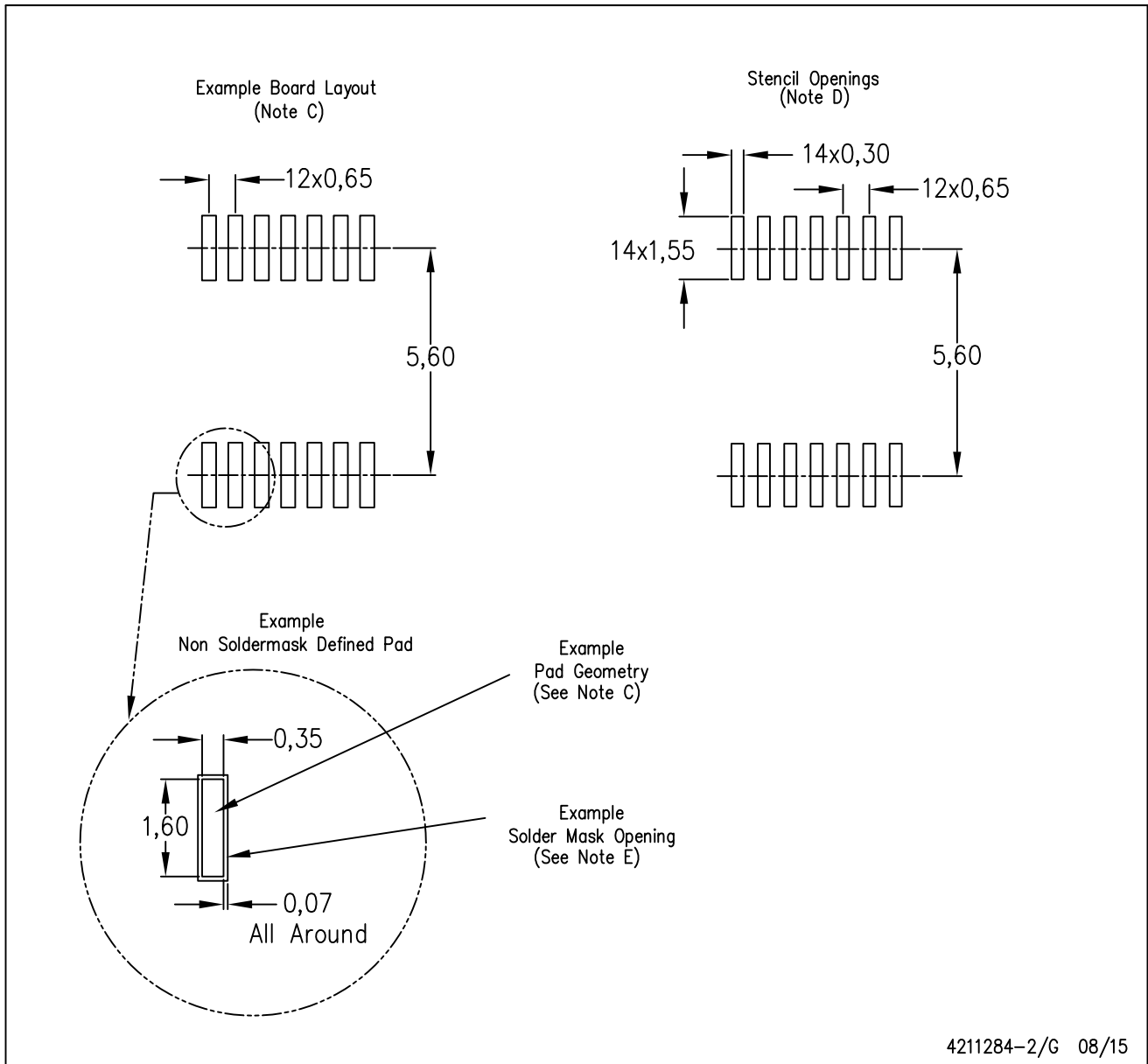
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

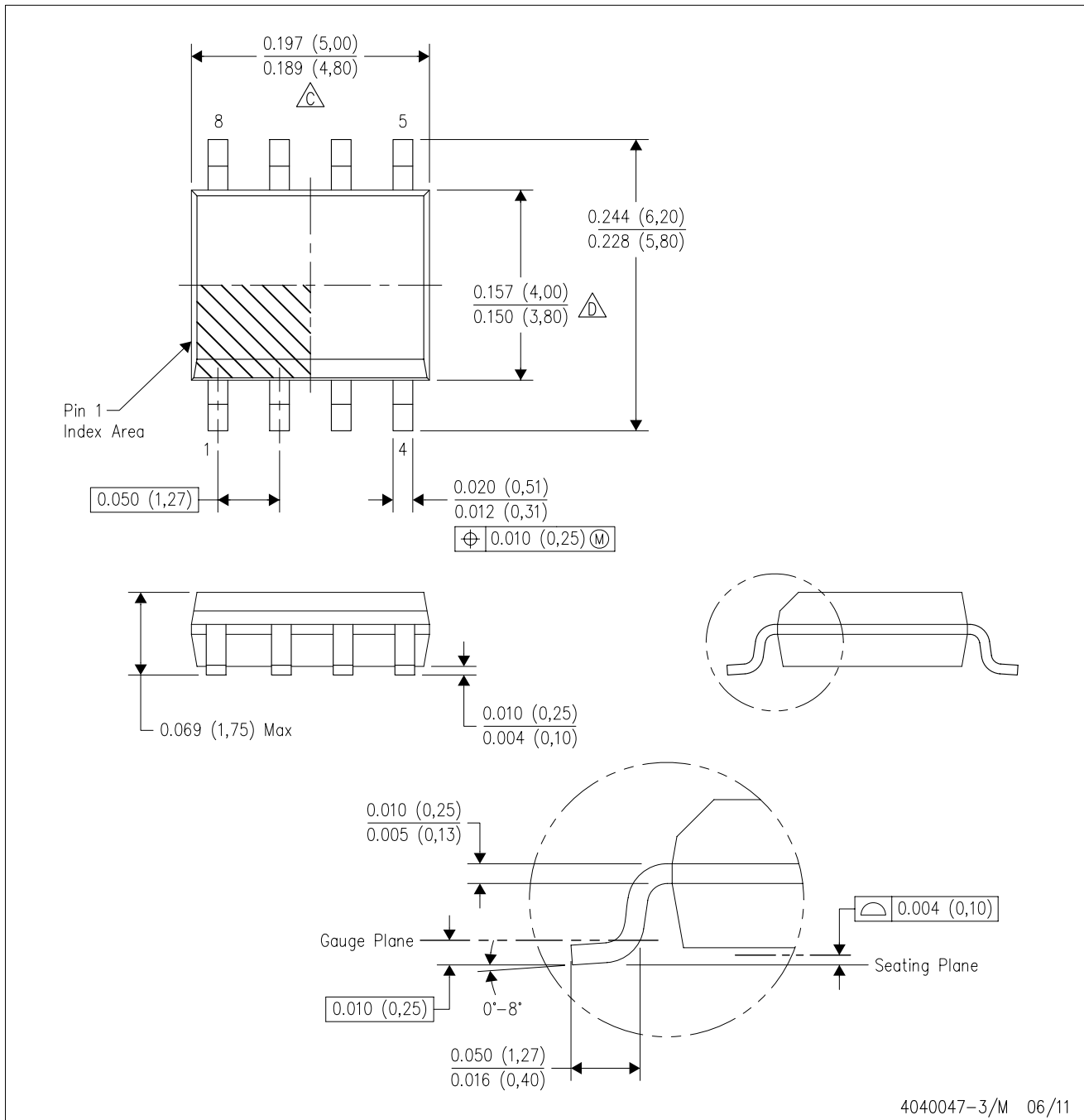


4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.





D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

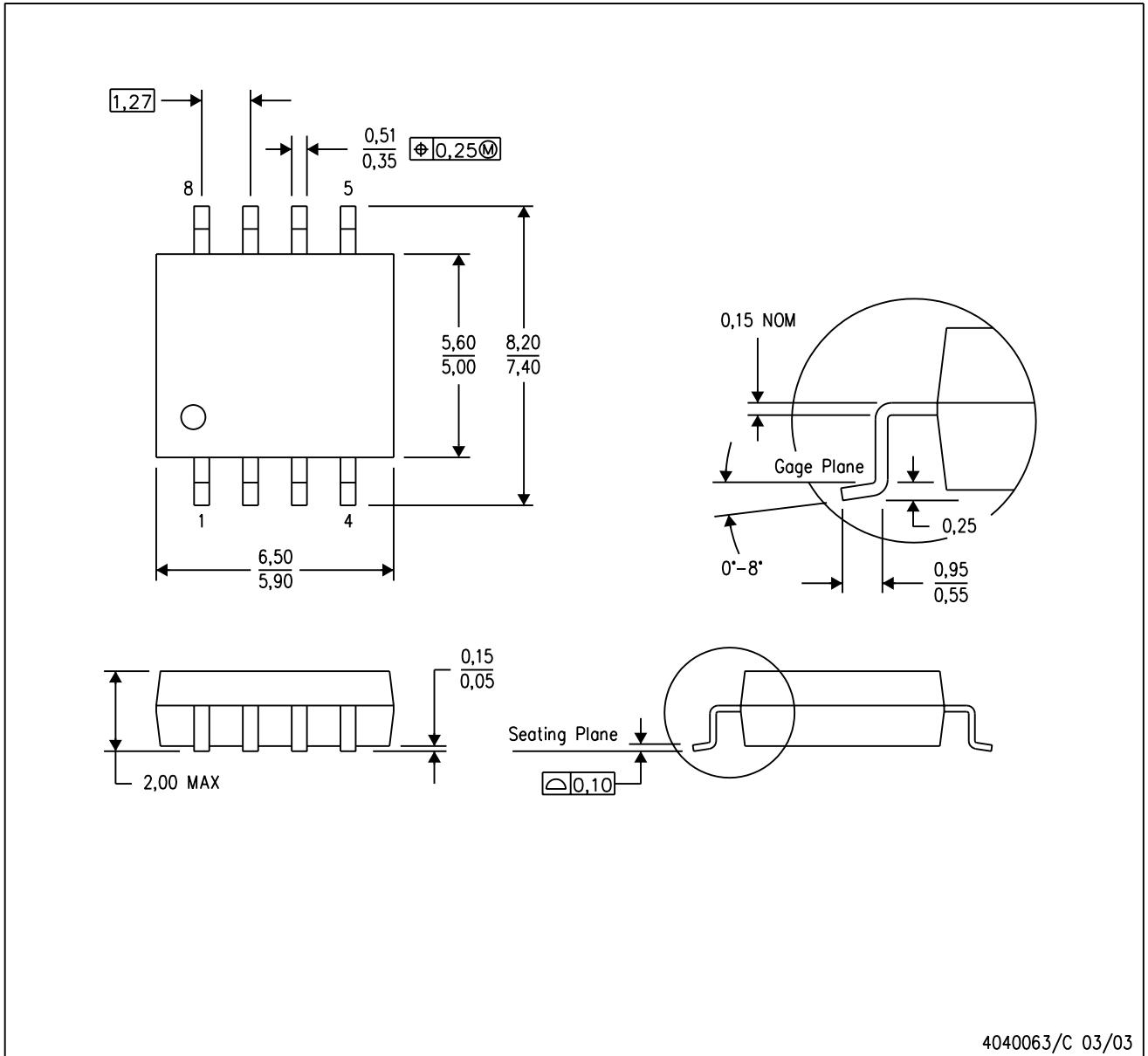
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

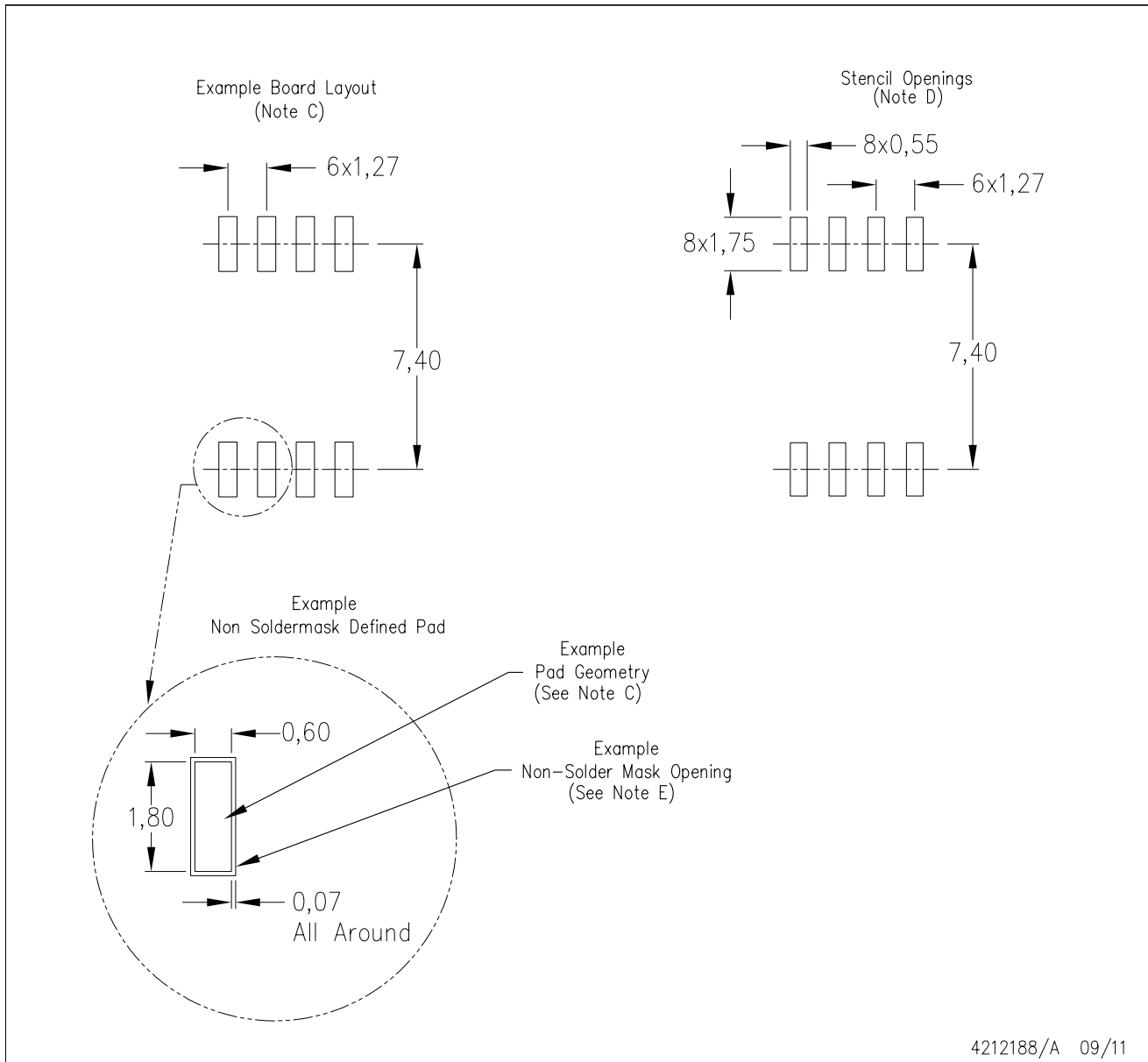
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

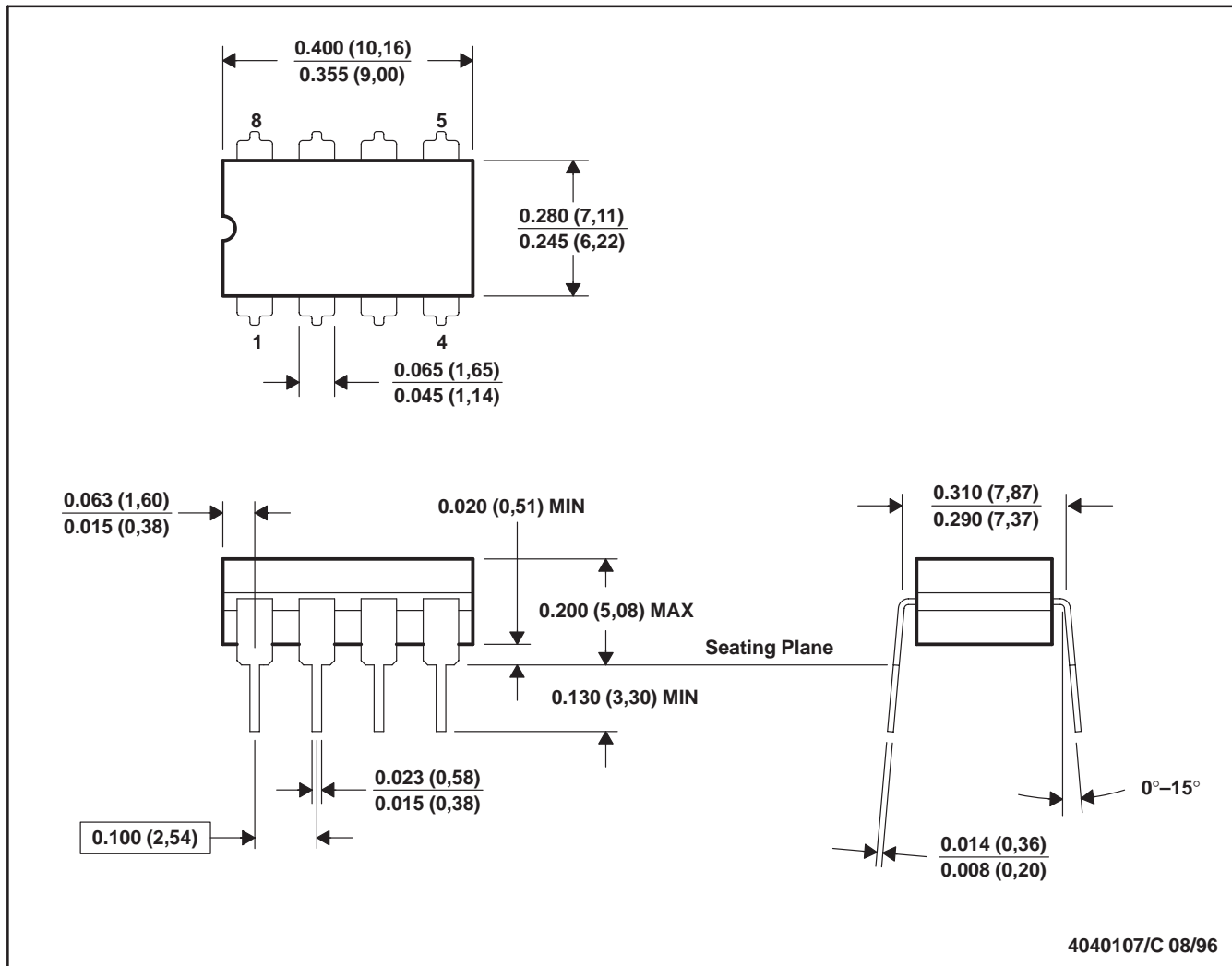
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



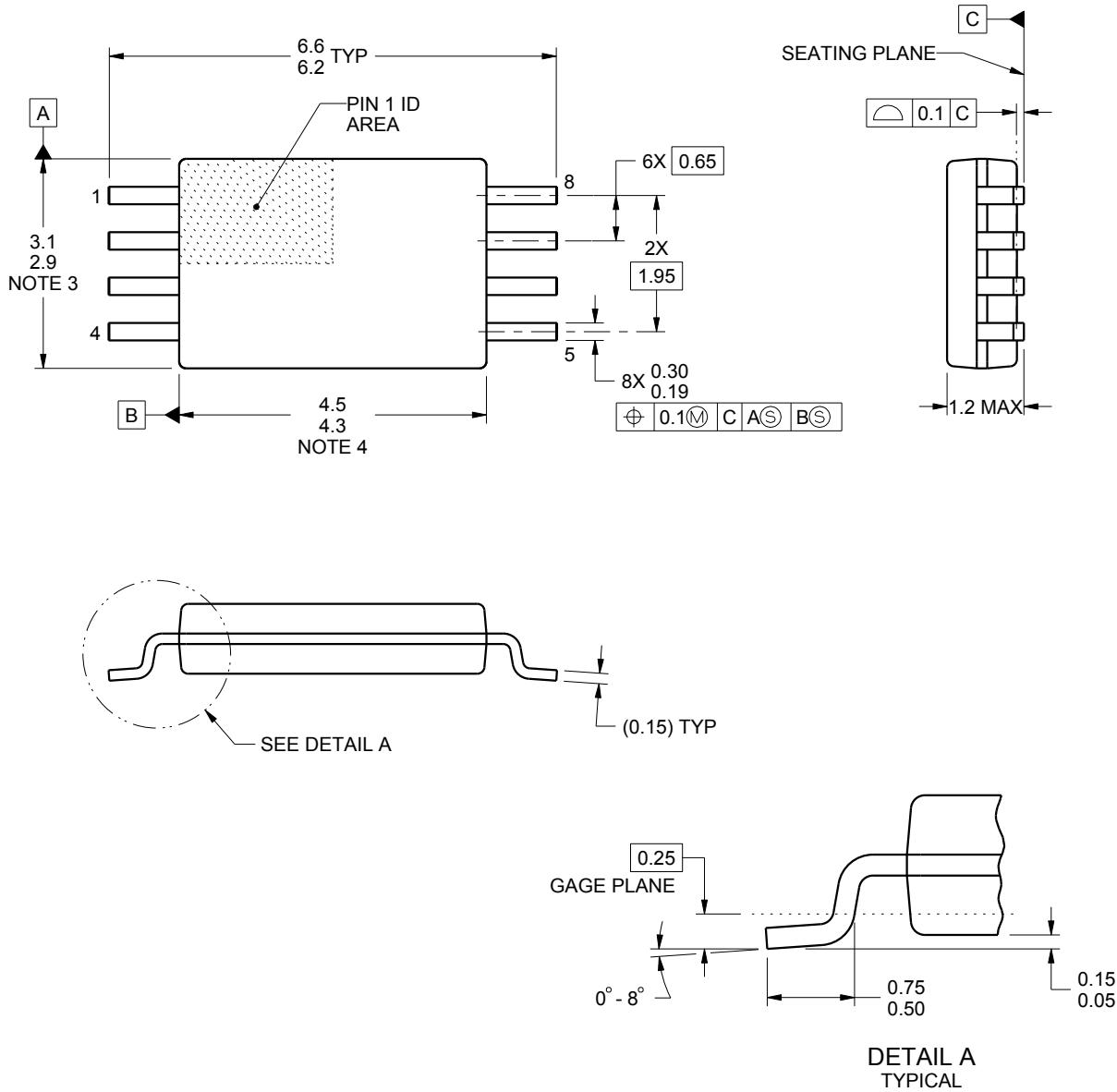
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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